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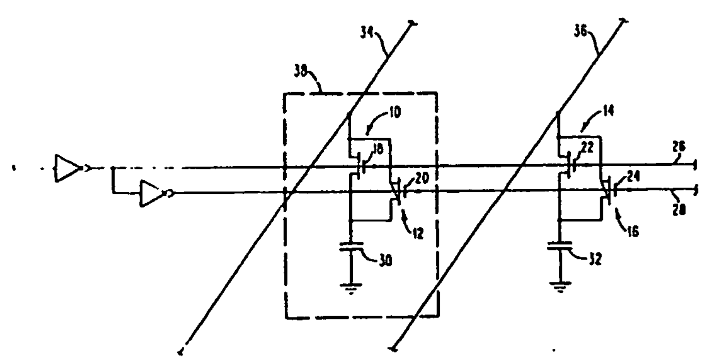
(54) CMOS-transistor and one-capacitor dram cell and fabrication process therefor.

(57) A complementary MOS one-capacitor dynamic RAM cell (e.g. 38) operates with a non-boosted wordline without a threshold loss problem. It includes one storage capacitor (30) and n- and p-type transfer devices (10, 12) connected to the storage capacitor which function as two complementary transistor devices having gates controlled by complementary signals on the RAM wordlines (26, 28).

FIG. 1



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tion of the structure of a CMOS memory cell according to the principles of the present invention.

Figs. 3 and 4 are schematic cross-sectional illustrations of the structure of the CMOS cell of Fig. 2 at certain steps within the fabrication process therefor.

Fig. 5 is a schematic cross-sectional illustration of another embodiment of a CMOS memory cell according to the principles of the present invention.

In integrated circuit technology employing dynamic-random-access-memory (DRAM) cells, as the DRAM density increases, it is important to scale down the area occupied by the DRAM cells, such as the one-transistor and one-capacitor DRAM device. A general dilemma in scaling down the transfer device in the DRAM cell is that in order to minimize the leakage through an "off" device, it is desirable to have a higher threshold voltage; but conversely, in order to maximize the stored charge and to obtain a higher charge transfer rate, it is desirable that the threshold voltage be small. The conventional way of using a boosted word line to avoid this problem becomes more difficult as the device dimensions are scaled down; for example, the reduced breakdown voltage of the scaled down device limits the possible boosted wordline voltage level. It is important for DRAMS, therefore, to design a new cell which allows using a non-boosted wordline, but without suffering the threshold loss problem as described.

The present invention provides a Complementary MOS one-capacitor DRAM cell (CMOS-1C cell) which overcomes the described problem. A circuit schematic of an embodiment of the new cell is shown in Fig. 1. The difference from the conventional one-transistor DRAM cell is that instead of having only a single type of transfer device connected to the storage capacitor, there are both an n- and a p-type transfer device in each cell, for example, devices 10,12 and 14,16 in Fig. 1. The gates 18,22 and 20,24 of these complementary devices are controlled by complementary word lines 26 and 28, respectively. At standby, the wordline 26 is low which turns off n-type devices 10,14 and the complementary wordline 28 is high which turns off p-type devices 12,16. For cell 38 which is comprised of the transfer devices 10 and 12, and the storage capacitor 30, the charge is stored on the capacitor 30, isolated from the bitline 34 at standby. When the cell is selected, wordline 26 goes high and complementary wordline 28 goes low to turn on both devices 10 and 12. Complementary devices 10 and 12 comprise a CMOS pass gate, having no threshold loss. As a result, there is no need to boost the wordline voltage level in order to store the full voltage, either the full power supply voltage VDD or zero volts. As a result, the total sense charge can be read from, or stored into, the capacitor 30 through the bitline 34 in a full-VDD amount, i.e., with no threshold loss.

There are several advantages of the described cell: (1) It does not suffer the threshold voltage loss for the charge transfer, even though the wordline voltage level is not boosted, because either VDD or zero can be fully transferred through the PMOS or NMOS, respectively; (2) the signal development is faster because both devices conduct most of the time during charge transfer; and (3) because the cell does not suffer threshold loss and has high charge transfer rate, the transfer devices can be designed to have large absolute values of the threshold voltage in order to suppress leakage.

The present invention provides a fabrication process which overcomes the technological difficulty of how to achieve both PMOS and NMOS devices within the area on the integrated circuit presently occupied by a single device. The present invention also provides a novel cell structure for the CMOS-1C cell, which occupies about the same area as the one-device cell.

Fig. 2 shows a schematic of the cross section of this new cell structure. The CMOS-1C cell of Fig. 2 includes a PMOS device having p+ drain and source regions 40,42, respectively, in n-well 44, and a gate 46. The cell also includes a trench capacitor 48 in a p+ substrate 50. The trench capacitor 48 is connected to the p+ source region 42 of the transfer device through a layer of interconnection 52 called the strap. The strap material, for example, may be titanium silicide, titanium nitride/titanium silicide, or cobalt silicide. Above the PMOS transfer device is the other, n-type, (NMOS) transfer device including source and drain regions 54,56, made in a SOI (silicon-on-insulator) film. Because the strap 52 is conductive to both p- and n-type material, the source and drain regions 42,40 and 54,56 of both NMOS and PMOS devices are connected. Gates 18 of the NMOS device and 20 (also referred to as 46) of the PMOS device are connected, respectively, to wordlines 26 and 28 which are connected to their own individual wordline drivers at the end of the array. The NMOS device and PMOS device of Fig. 2 correspond to devices 10 and 12 of Fig. 1, respectively, and operate as previously described.

A process to fabricate the cell structure of Fig. 2 will be described. Although the process will be described for one cell, it should be understood that the process applies to the fabrication of a plurality of cells in a dense array. The process consists of the following steps:

Step (1) With a p epitaxial layer 58 disposed on a p+ semiconductor substrate 50, Reactive Ion Etch (RIE) a 5 to 6μm deep trench into the p epi layer 58 and p+ substrate wafer 50. (Fig. 3)

and read out from said storage capacitor in response to said NMOS and PMOS type transistor devices being turned on and off by said signals on said wordlines.

2. The memory cell according to claim 1 wherein said first electrodes of said NMOS type transistor device is a source electrode and said first electrode of said PMOS type transistor device is a drain electrode, and said second electrode of said NMOS type transistor device is a drain electrode and said second electrode of said PMOS type transistor device is a source electrode.

3. The memory cell according to claim 1 wherein said first electrode of said NMOS type transistor device is a drain electrode, and said second electrodes of said NMOS type transistor device is a source electrode, said first electrode of said PMOS type transistor device is a source electrode, and said second electrode of said PMOS type transistor device is a drain electrode.

4. The memory cell according to claims 1 or 2 including a semiconductor substrate (e.g. 50 in Fig. 2),
an epitaxial silicon layer (58) disposed on said substrate,
an n-well region (44) provided, preferably implanted, in said epitaxial layer,
a polysilicon filled trench (60) disposed in said substrate and epitaxial layers and insulated therefrom to form said storage capacitor (48),
said PMOS type transistor device disposed on said epitaxial layer and including source and drain impurity regions provided, preferably implanted, into said n-well region and an oxide covered gate electrode disposed over said n-well region proximate to said source and drain regions,
said NMOS type transistor device vertically disposed over said PMOS type transistor device and including source and drain impurity regions disposed over and electrically connected to said source and drain regions of said PMOS type transistor device, and, an oxide covered gate electrode disposed over and electrically isolated from said gate electrode of said PMOS type transistor device.

5. The memory cell according at least to claim 4 further including a layer (e.g. 52 in Fig. 2) of conductive material disposed over said polysilicon filled trench, over said source region of said PMOS type transistor device and beneath said source region of said NMOS type transistor device to electrically connected said trench storage capacitor to said source regions.

6. The memory cell according at least to claim 4 or 5 wherein said substrate is composed of p+ type silicon, said epitaxial silicon layer is p type, said polysilicon filled in said trench is p+ type, said n-well is composed of a phosphorous implant and said source and drain regions of said PMOS and NMOS type transistor devices are formed of phosphorus and boron implants to provide graded source/drain junctions.

7. The method for fabricating a memory cell for a semiconductor memory array comprising the steps of:

Step (1) dispose an epitaxial layer on a semiconductor substrate and reactive ion etch a trench into the said epitaxial layer and substrate,

Step (2) form a composite oxide/nitride/oxide storage insulator layer on the walls inside said trench,

Step (3) fill said trench with polysilicon and planarize,

Step (4) form a retrograde n-well in said epitaxial layer by a surface impurity implant and a deep impurity implant,

Step (5) grow gate oxide and deposit polysilicon gate material for a PMOS type device and deposit an oxide film insulator layer over the PMOS gate and lithographically pattern said oxide film layer,

Step (6) implant dopants into said n-well to provide graded source/drain junctions for PMOS and NMOS transistor devices, respectively,

Step (7) open the surfaces of said source/drain regions for silicide formation wherein said gate element is protected from said silicide by said oxide film insulator layer formed in step (5),

Step (8) form a lightly doped silicon film over said silicide, gate oxide and isolation regions wherein said lightly doped silicon film is deposited in polycrystalline structure and recrystallized by beam annealing,

Step (9) define the NMOS type transistor device active area and grow thin NMOS gate oxide,

Step (10) adjust channel threshold voltages by an impurity implant.

Step (11) deposit polysilicon NMOS type transistor device gate material and pattern,

Step (12) form oxide spacer regions on said NMOS gate electrode edges,

Step (13) implant dopants to obtain source/drain junctions for a transfer device and grow oxide to cover the device.

8. The method for fabricating a memory cell according to Claim 7 wherein said substrate is composed of p+ type silicon, said epitaxial silicon layer is p type, said polysilicon filled in said trench in step (3) is p+ type, said n-well formed in step (2) is composed of a phosphorous implant and said source and drain regions of said PMOS and NMOS type transistor devices are formed of phosphorus and boron implants to provide graded source/drain junctions.

9. The method of fabricating a memory cell according to claims 7 or 8 wherein said lightly

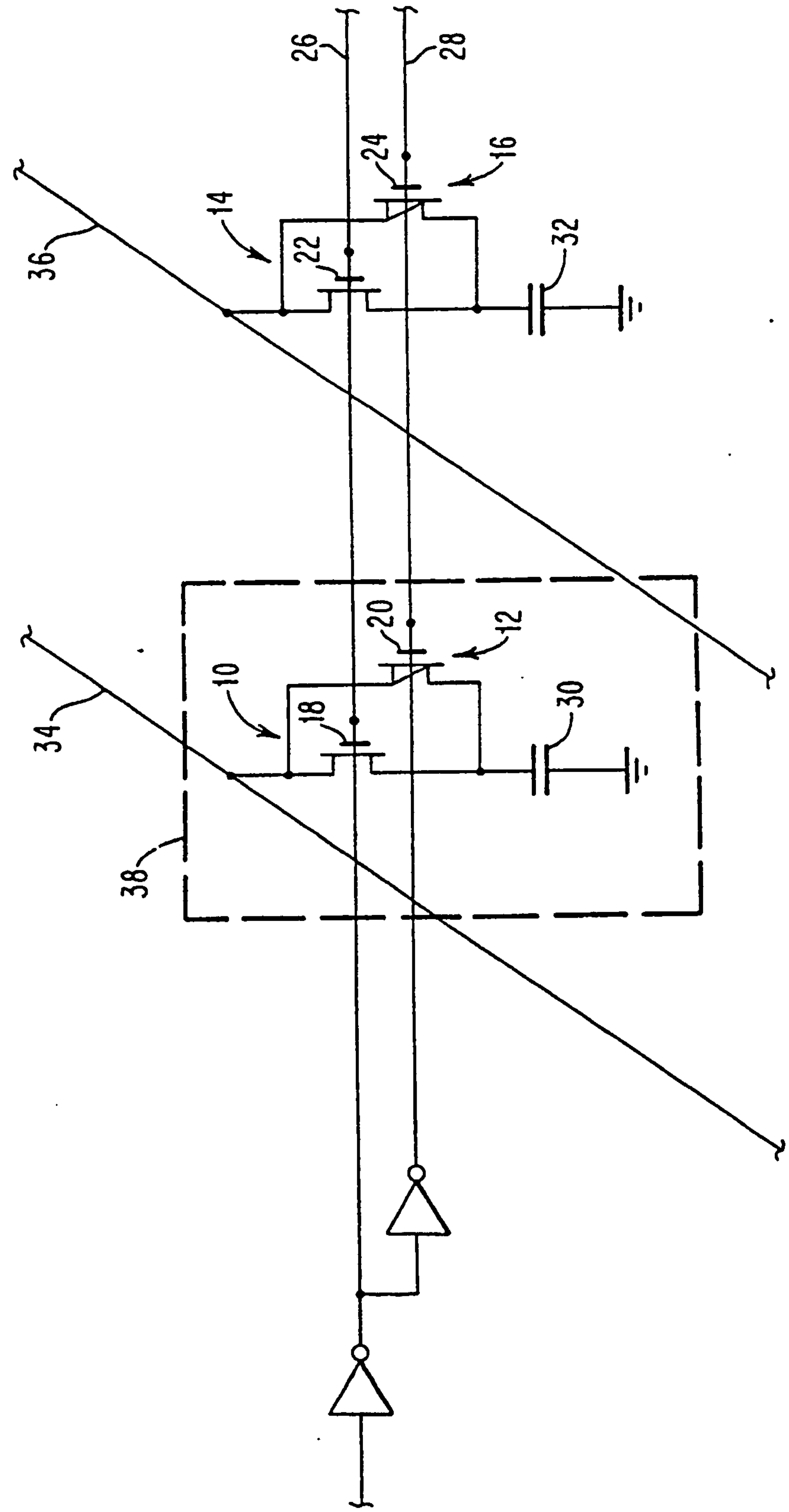


FIG. 1

FIG. 3

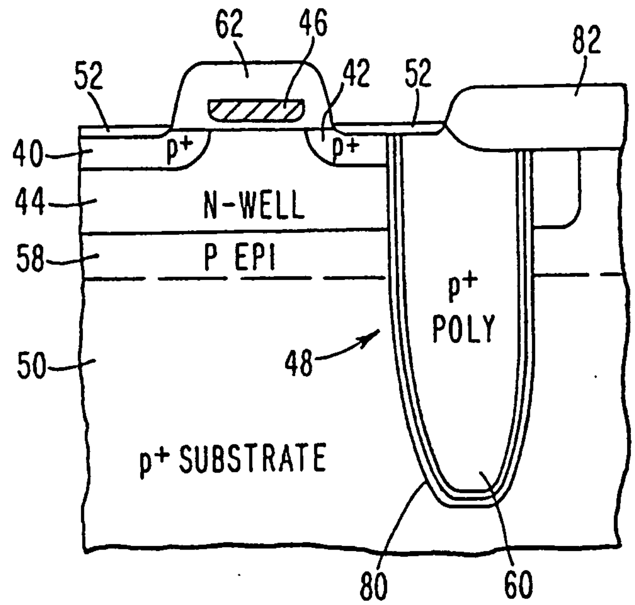
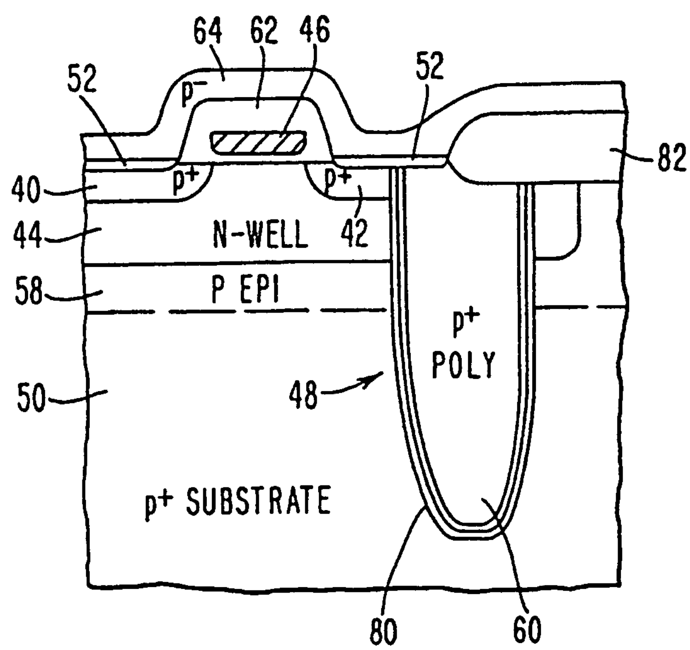

62
46
82
52
42
52
40
p+
p+
44
N-WELL
58
P EPI
p+
POLY
48
50
p+ SUBSTRATE
80
60

FIG. 4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